High Power Consumption Mode of Optical Module

Overview

We explained how AC-coupling UBB SiCaps are efficient in very high-speed optical modules, thanks to their specific design and low profile.

Key Takeaways

High power consumption in optical modules is primarily driven by high data rates, signal processing requirements, and thermal constraints, with solutions focusing on efficient design, miniaturized power modules, and optimized pluggable optics. Causes of High Power Consumption1. Data Rate and Signal Processing: Modern optical modules support extremely high data rates, such as 400 Gbps and 800 Gbps, which require more current to power clock and data recovery (CDR), gearbox, and digital signal processor (DSP) chipsets.

These components consume significant energy to process large volumes of data while maintaining signal integrity within tight thermal budgets. 2.

Ser

Des Losses: The electrical signal path from the host ASIC to the optical interface introduces losses proportional to the lane length.

Longer Ser

Des lanes require more DSP power to correct distortions, increasing overall module power consumption. 3. Form Factor Constraints: Standardized form factors like QSFP-DD and OSFP limit the available space and thermal dissipation.

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High-performance modules must fit within these constraints, which can increase power density and heat generation. 4. Reach and Technology: Long-reach modules (e.g., ZR, ER) and coherent optics require more powerful lasers and electronics, further increasing energy usage.

Short-reach modules consume less power but still face efficiency challenges at high speeds. Strategies to Reduce Power Consumption1. Efficient Capacitors: Using ultra broadband silicon capacitors (SiCaps) instead of traditional MLCCs reduces insertion loss and crosstalk, improving signal integrity and lowering energy requirements for high-speed optical modules.

2. Miniaturized Power Modules: Compact, synchronous step-down power modules, such as Renesas RAA210040 and RAA210030, provide high current in a small footprint with low dropout voltage and fast transient response. These modules optimize power delivery while minimizing losses in space-constrained optical modules.

3. Optimized Pluggable Optics: Reducing SerDes lane length or count, and using high-efficiency pluggable optics for intra-data center connectivity, lowers DSP workload and power consumption. Fully retimed optics (FRO) can improve performance but may increase power; careful design balances energy efficiency and signal integrity.

4. Thermal Management: Lowering power consumption reduces heat output, easing cooling requirements and enabling higher port densities without exceeding rack power limits. 5.

Design Trade-offs: Engineers must balance data rate, reach, and power efficiency. Techniques like higher-order modulation and carrier frequency optimization can increase throughput but require careful management of SNR and DSP power.

Conclusion

High power consumption in optical modules arises from the combination of high-speed data processing, electrical losses, form factor limitations, and thermal constraints. Addressing these challenges involves efficient component selection, miniaturized power modules, optimized pluggable designs, and careful thermal management, enabling data centers to scale bandwidth while controlling energy usage and operational costs.

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Article Content

HOW TO REDUCE POWER CONSUMPTION IN HIGH-SPEED

We explained how AC-coupling UBB SiCaps are efficient in very high-speed optical modules, thanks to their specific design and low profile. We also saw the impact of the SNR on the power consumption

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